

## PLASMA PROCESSING METHOD AND APPARATUS

### Field of the Invention

5           The present invention relates to a plasma processing method and apparatus; and, more particularly, to a method and apparatus for eliminating contaminants such as deposits accumulated on a wall surface and so on of a processing chamber during a plasma processing process.

10

### Background of the Invention

          Foreign substances attached on a substrate such as a semiconductor wafer during a manufacturing process of a semiconductor device result in pattern defects in the device, thereby lowering a manufacturing yield. Accordingly, a process employing plasma, e.g., dry etching and CVD, in a manufacturing process has been widely studied recently. Specifically, a plasma reaction of various gases introduced into a manufacturing apparatus is used to carry out micro processing, e.g., film deposition and etching.

20           In such a process, deposits (a deposition film) may be attached on an inner wall of the manufacturing apparatus, in addition to an object being micro-processed. Since, for example, molecules of an etching gas may be decomposed or combined with each other in the plasma and etching by-

products may be generated during the dry etching process, deposits thereof may be attached on the inner wall of the apparatus during the dry etching process. As the number of wafers treated increases, the deposits get thicker and are partially peeled off to generate dusts, which cause pattern defects in devices. Therefore, such deposits attached on the inner wall in the apparatus must be periodically removed.

If a depo-process is followed by a depoless-process in a same chamber while dry etching a silicon oxide film, an etching rate of the depoless-process becomes unstable, since the depoless-process can be easily influenced by deposits produced in the same chamber during the preceding depo-process. The term "depo-process" used herein denotes a process of using a gas with a smaller F/C (fluorine/chlorine) ratio, e.g.,  $C_4F_8$ , which leaves a visible amount of polymers including a CF based element such as  $CF_4$  attached to the chamber. The term "depoless-process" used herein denotes a process using a gas with a larger F/C ratio, e.g.,  $CF_4$ , which leaves no polymers attached to the chamber.

In order to solve the above problem, a gas reacting with the deposits is conventionally introduced to perform a dry cleaning process. Japanese Patent Laid-Open Publication No. 5-291213 discloses such a dry cleaning process scheme, wherein while a wafer installed on a supporting table is maintained at a temperature below  $0^\circ C$ , a process gas, i.e.,

a mixed gas of  $\text{CF}_4$  and  $\text{O}_2$ , is introduced into a chamber so that the deposits may be removed by an activated process gas. Japanese Patent Laid-Open Publication No. 7-78802 discloses another dry cleaning process scheme, wherein a cleaning gas  
5 in which  $\text{H}_2$  gas is added to  $\text{O}_2$  gas is introduced to perform the dry cleaning process.

The gas used in the dry cleaning process reacts with the deposits of deposition film to be removed to produce compounds of high vapor pressures, so that the deposits are  
10 removed by an evaporation and vacuum exhaustion. Since a condition in the chamber just after the dry cleaning process is different from a stable condition in the chamber reached after repeatedly performing the depoless-process, the etching rate in the depoless-process decreases.

15 To solve the above problem, a seasoning process has been introduced. In the seasoning process, instead of processing the wafer right after the dry cleaning process, a plurality of dummy wafers are transferred into the chamber and a plasma processing is performed on the dummy wafers  
20 under exactly same process conditions as those of the actual plasma processing process to stabilize the process conditions in the chamber.

However, the seasoning process requires the dummy wafers for the seasoning process and at least several  
25 minutes of processing time. Accordingly, an additional effort and an additional time needed therefore lower an

operating rate of a series of plasma processes.

#### Summary of the Invention

5           It is, therefore, an object of the present invention to provide a plasma processing method and apparatus capable of preventing a decrease in an etching rate of the depoleless-process without performing a seasoning process right after a dry cleaning process.

10           The inventor of the present invention rigorously conducted a series of experiments and found that decrease in the etching rate during the depoleless-process right after the dry cleaning process results from silicon-containing substances sputtered from silicon-containing materials, e.g.,  
15           a dummy wafer used in the dry cleaning process and a focus ring, and attached on the inner wall of the chamber. Further, the inventor found a dry cleaning process method, that prevents such sputtered substances of wafer from being left attached on the inner wall of the chamber.

20           In accordance with a preferred embodiment of the present invention, there is provided a plasma processing method having a first and a second plasma processing step carried out in a single chamber, wherein deposits are substantially accumulated in the chamber during first plasma  
25           processing step and substantially no deposits are accumulated in the chamber during the second plasma

processing step, the method comprising the step of:

dry cleaning an inside of the chamber by using a dummy substrate between the first and the second plasma processing step,

5            wherein the dry cleaning step is performed by supplying into the chamber a deposit removing gas for removing the deposits produced in the chamber during the first plasma processing step and a dummy substrate etching gas capable of etching the dummy substrate.

10           Further, the deposit removing gas is preferably a gas capable of reacting with deposits of deposition film to be removed to produce compounds of high vapor pressures. Specifically, an oxygen gas, a nitrogen gas, a hydrogen gas, an ammonia gas or a combination thereof is used as the  
15           deposit removing gas.

             Furthermore, the dummy substrate etching gas is preferably a gas capable of reacting with and etching the wafer, i.e., a CF-based gas, a CHF-based gas or a SF-based gas.

20           In accordance with another preferred embodiment of the present invention, there is provided a plasma processing method comprising the steps of:

             performing a plasma processing on an object to be processed in a chamber;

25           after the step of performing the plasma processing, dry cleaning an inside of the chamber by using a dummy

substrate,

wherein the dry cleaning step is performed by supplying into the chamber a deposit removing gas for removing deposits produced in the chamber during the step of performing the plasma processing and a dummy substrate etching gas capable of etching the dummy substrate, and

wherein a ratio of a flow rate of the dummy substrate etching gas to that of the deposit removing gas is not less than about 0.14% but not larger than about 7.1%.

Further, it is preferable that the high frequency power applied to one of the top and the bottom electrode during the step of performing the plasma processing ranges from about  $3.18 \text{ W/cm}^2$  to about  $4.78 \text{ W/cm}^2$ .

Furthermore, it is preferable that the dry cleaning step is performed between a first and a second plasma processing step carried out in a same chamber, wherein deposits tend to be attached to the chamber during the first plasma processing step and deposits are not likely left attached to the chamber during the second plasma processing step.

Since a silicon containing material, e.g., silicon dioxide, is not going to be attached on the inner wall of the chamber during the dry cleaning process in accordance with the present invention, the decrease in the etching rate in the depossess-process carried out right after the dry cleaning process can be prevented and thus the seasoning

process need not be performed right after the dry cleaning process. As a result, additional effort and time required for the seasoning process can be saved and the operating rate of a series of plasma processes can be enhanced.

5

#### Brief Description of the Drawings

The above and other objects and features of the present invention will become apparent from the following  
10 description of preferred embodiments given in conjunction with the accompanying drawings, in which:

Fig. 1 shows a schematic cross sectional view of a plasma processing apparatus in accordance with a preferred embodiment of the present invention;

15 Figs. 2A to 2D illustrate graphic illustration explaining variations of etching rate and in-surface uniformity during a depeless-process executed after a dry cleaning process in accordance with the present invention;

Fig. 3 represents a schematic cross sectional view of  
20 an experimental apparatus for analyzing deposits attached on a surface of a chip of yttrium oxide after a dry cleaning process in accordance with a preferred embodiment of the present invention;

Fig. 4 outlines an XPS analysis on a surface of a chip  
25 of yttrium oxide to analyze deposits attached on the surface of the chip of yttrium oxide after a conventional dry

cleaning process;

Fig. 5 depicts another XPS analysis on a surface of a chip of yttrium oxide to analyze deposits attached on the surface of the chip of yttrium oxide after the conventional dry cleaning process and a depoleless-process;

Fig. 6 describes an XPS analysis on a surface of a chip of Yttrium oxide to analyze deposits attached on the surface of the chip of yttrium oxide after a dry cleaning process in accordance with a preferred embodiment of the present invention;

Figs. 7A to 7C present graphic illustration explaining variations of etching rate and in-surface uniformity of etching rate during the depoleless-process after carrying out conventional dry cleaning process and a dry cleaning process in accordance with the present invention for 30 minutes;

Figs. 8A to 8D explain graphic illustration explaining the examination results of variations of etching rate and in-surface uniformity of etching rate during a depoleless-process after a dry cleaning process in accordance with the present invention is performed while varying an added amount of  $\text{CF}_4$ ;

Fig. 9 depicts a schematic cross sectional view of an experimental apparatus for examining variations of etching rate depending on a variety of conditions applied during the dry cleaning process;

Fig. 10 is a table explaining a relationship between



the presence of  $\text{CF}_4$  added and an ashing rate ( $\text{\AA}/\text{min}$ ) at various locations in an experimental chamber;

Fig. 11 is a table for illustrating a relationship between a power applied to a bottom electrode and time (second) required to remove deposits attached to resist chips at various locations in the experimental chamber 300 after performing the depo-process on 25 wafers with processing time of 3 min/wafer;

Fig. 12A is a flow chart of a plasma processing method in accordance with the present invention; and

Fig. 12B is a flow chart of a conventional plasma processing method.

#### Detailed Description of Preferred Embodiments

15

Hereinafter, a preferable embodiment of the present invention will be described in detail with reference to the accompanying drawings. In the specification and the drawings, parts whose functions and structures are substantially identical with each other will be assigned with a similar reference numeral to avoid redundant explanation.

Fig. 1 illustrates a cross sectional view of a plasma processing apparatus 100 in accordance with a first embodiment of the present invention. The plasma processing apparatus 100 has a sealed chamber 102. The chamber 102 is

a stepped cylindrical chamber which has an upper part 102a with a smaller diameter and a lower part 102b with a larger diameter. The chamber 102 has a wall made of aluminum whose surface is coated with an yttrium oxide ( $Y_2O_3$ ) film with a thickness of about 200  $\mu m$ , for example. The chamber 102 is electrically grounded.

A supporting table 104 is installed in the chamber 102. The supporting table 104 horizontally supports an object to be processed, e.g., a semiconductor wafer W (referred to as a wafer, hereinafter) with a diameter of 200 mm. The supporting table 104 is made of, e.g., Al and supported by a support 108 through an insulating plate 106. A focus ring 110 is disposed around an upper periphery of the supporting table 104. The focus ring 110 is made of a conductive material, e.g., single crystal silicon.

The supporting table 104 and the support 108 move upwards and downwards by a ball screw mechanism having ball screws 112. A bellows 114 made of stainless steel covers a driving portion under the support 108. A bellows cover 116 surrounds the bellows 114.

The supporting table 104 constituting a bottom electrode is coupled to an RF power supply 120 through a matching box 118. A 13.56 MHz high frequency power is applied from the RF power supply 120 to the supporting table 104, for example. Installed over the supporting table 104 is a shower head 122 constituting a top electrode. The

supporting table 104 faces the shower head 122 in a parallel manner. The shower head 122 is grounded. The supporting table 104 (bottom electrode) and the shower head 122 (top electrode) serve as a pair of electrodes.

5           An electrostatic chuck 124 is installed on the supporting table 104 to attract the wafer W thereto with electrostatic force. The electrostatic chuck 124 includes an insulator 124b and an electrode 124a embedded therein. A power supply 126 is connected to the electrode 124a. With  
10 the application of a voltage from the power supply 126 to the electrode 124a, the wafer W is adhered to the electrostatic chuck 124 by a Coulomb force.

          There is formed a coolant channel (not shown) inside the supporting table 104 through which an appropriate  
15 coolant to control the temperature of the supporting table 104 circulates. Further, a backgas supply structure (not shown) for supplying an inert gas, e.g., a He gas, to increase the thermal conductivity between the supporting table 104 and the wafer W is provided in the supporting  
20 table 104 and the electrostatic chuck 124. Heat is transferred between the supporting table 104 and the wafer W to maintain the wafer W at a required temperature. Installed outside of the focus ring 110 is a baffle plate 128. The baffle plate 128 is connected to the chamber 102  
25 through the support 108 and the bellows 114.

          Installed at a ceiling portion of the chamber 102 is

the shower head 122 facing the supporting table 104. The shower head 122 has a plurality of gas inlet holes 130 in a bottom side thereof and a gas inlet 132 on a top side thereof. A space 134 is formed within the shower head 122.

5 The gas inlet 132 is coupled with a gas supply line 136. Another end of the gas supply line 136 is connected to a process gas supply system 138 for supplying a process gas, which includes a reaction gas for plasma processing, e.g., etching, and a dilution gas. For example, as conventionally

10 used in the prior art, a halogen gas may be used as the reaction gas while an Ar gas, a He gas and the like may be used as the dilution gas.

The process gas from the process gas supply system 138 is provided to the space 134 of the shower head 122 through

15 the gas supply line 136 and the gas inlet 132, and then is injected from the gas inlet holes 130 to etch a film formed on the wafer W.

Installed at a sidewall in the lower part 102b of the chamber 102 is a gas outlet port 140. The gas outlet port

20 140 is connected to a gas pumping system 142. By operating a vacuum pump (not shown) installed in the gas pumping system 142, the chamber 102 may be depressurized to a certain vacuum level. Installed at a top sidewall of the lower part 102b is a gate valve 144 to open and close an

25 opening for transferring the wafer W.

Concentrically arranged around the upper part 102a of

the chamber 102 is a dipole ring magnet 146 as a means for generating a magnetic field in a region between the supporting table 104 and the shower head 122. The dipole ring magnet 146 is configured to be rotated by using a rotating unit (not shown), e.g., a motor.

In the plasma processing apparatus of the above-described configuration, the gate valve 144 is first opened to carry the wafer W in the chamber 102. The wafer W is mounted on the supporting table 104 and the gate valve 144 is closed. The supporting table 104 moves upwards to a position shown in Fig. 1 and the chamber 102 is exhausted through the gas outlet port 140 by the vacuum pump of the gas pumping device 142.

After the chamber 102 reaches to a required vacuum level, a certain process gas is introduced from the process gas supply system 138 to the chamber 102 so that the chamber 102 can be maintained at a given pressure, e.g., 40 mTorr. Then, a high frequency power with a frequency of, e.g., 13.56 MHz and a power of, e.g., 1000 to 5000 W is applied from the RF power supply 120 to the supporting table 104. At this time, a predetermined voltage is applied from the DC power supply 126 to the electrode 124a of the electrostatic chuck 124, so that the wafer W is attracted to be adhered to the electrostatic chuck 124 by the Coulomb force.

As the high frequency power is applied to the bottom electrode, i.e., the supporting table 104 as described above,

an electric field is generated between the top electrode, i.e., the shower head 122, and the bottom electrode, i.e., the supporting table 104. Further, since the dipole ring magnet 146 generates a horizontal magnetic field at the upper part 102a of the chamber 102, a magnetron discharge due to electron drift is generated in a processing region where the wafer W is located, which in turn generates a plasma from the process gas so that a film formed on the wafer W can be etched away.

Hereinafter, variations of etching rate in a depoless-process carried out after the dry cleaning process will be described.

Referring to Figs. 2A to 2D, there is shown a graphic illustration for describing variations in an etching rate and those in an in-surface uniformity of etching rate, i.e., a variation in the uniformity of etching rate within the surface, for cases where 25 wafers were processed by the depoless-process after the dry cleaning process. The vertical axes in graphs on the upper side represent an etching rate ( $\text{\AA}/\text{min}$ ); those on the lower side, an in-surface uniformity of etching rate (%); and the horizontal axes, an elapsed time (min) measured from the time of the termination of the dry cleaning process. The processing time of the depoless-process is about 1 minute per a wafer W and the number in the horizontal axis corresponds to the number of wafers processed by the depoless-process.

In Figs. 2A to 2D, the processing durations for the dry cleaning process are 3, 5, 10 and 30 minutes, respectively.

Values shown in each graph denotes an average and a standard deviation of an etching rate or an in-surface uniformity after the etching rate or the in-surface uniformity during the depoless-process reaches a stable range. The stable ranges were determined based on the criteria that the etching rates and the in-surface uniformities respectively remain within  $\pm 1.0 \%$  and  $\pm 3.0 \%$  with respect to an average of the etching rates and an average of the in-surface uniformities after reaching their respective stable regions. The dotted portions in Figs. 2A to 2D represent unstable regions.

An exemplary processing condition of the depoless-process for plasma-etching a thermal silicon oxide film formed all over the surface of the wafer, i.e., an object to be processed, with a diameter of 200 mm is processed by plasma etching is as follows:

a pressure in the chamber; 45 mTorr,

a high frequency power applied to the bottom electrode and time during which the high frequency power is applied; 1400 W and 1 minute, respectively,

flow rates of  $\text{CF}_4$ ,  $\text{O}_2$  and Ar gases in a mixed gas thereof supplied as the process gas; 80 sccm, 20 sccm and 160 sccm, respectively,

temperatures of the top electrode, the sidewall of the chamber and the bottom electrode; 60°C, 60°C and 40°C, respectively, and

pressure levels of the backgas (He); 7 Torr in a central region of the object to be processed and 40 Torr in a peripheral region thereof.

The 1st, 2nd, 3th, 5th, 7th, 10th, 15th, 20th and 25th processed wafers respectively had thermal silicon oxide layers formed thereon while the other wafers were dummy wafers with surfaces thereof coated with resist films, respectively.

An exemplary processing condition for the dry cleaning process were as follows:

a pressure in the chamber;.100 mTorr,  
a high frequency power applied to the bottom electrode and time during which the high frequency power is applied; 2000 W and 1 minute, respectively,

a flow rate of O<sub>2</sub> gas supplied as the process gas; 700 sccm,

temperatures of the top electrode, the sidewall of the chamber and the bottom electrode; 60°C, 60°C and 40°C, respectively, and

pressure levels of a backgas (He); 7 Torr in the central region of the object to be processed and 40 Torr in the peripheral region thereof. The silicon dummy wafers were used during the dry cleaning process.



The variations in the etching rate and those in the in-surface uniformity during the deprocess after executing the dry cleaning process under the above condition will be described. As the dry cleaning process time increases from 3 minutes to 30 minutes, the etching rate decreases and the in-surface uniformity increases slightly at the time of the termination of the dry cleaning process. Further, as the dry cleaning process time increases from 3 minutes to 30 minutes, the time required for the etching rate and the in-surface uniformity to be stabilized from the time of the termination of the dry cleaning process increases from 1-2 minutes to 9 minutes. From the above results, it can be seen that the drop of the etching rate at the time of the termination of the dry cleaning process and the time required to reach a stable etching rate from the time of the termination of the dry cleaning process depend on the time duration during which the dry cleaning process is performed.

Experiments carried out to examine a variation of etching rate of the dry cleaning process will now be described. Specifically, a chip 200 was prepared first by thermally spraying yttrium oxide ( $Y_2O_3$ ) on a surface of an Al member whose material was identical with that of the chamber 102 used in the preferred embodiment of the present invention and the chip 200 was placed in an experimental chamber 202 shown in Fig. 3 in which a dry cleaning process

was carried out under the processing condition described below. After the dry cleaning process, the components of the deposits attached on the surface of the chip 200 were examined by X-ray photoelectron spectroscopy (XPS). The  
5 chip 200 is fixed on a ceiling portion 204 of the experimental chamber 202 by using a silicone tape (not shown) which has a good thermal conductivity.

As in the plasma processing apparatus 100 used in the preferred embodiment of the invention, a wafer W was mounted  
10 on a supporting table 206 and a focus ring 208 was disposed around an upper periphery of the supporting table 206 to concentrate plasma in a processing space S. The focus ring 208 was made of a conductive material, e.g., single crystal silicon. Installed on the lower portion of the experimental  
15 chamber 202 was a baffle plate 210.

In the experiments, XPS was used to analyze the components of deposits attached on the surface of the chips 200 obtained in the experimental chamber 202 under 3 processing conditions as follows:

- 20 (1) a dry cleaning process for 15 minutes,  
(2) a dry cleaning process for 15 minutes and, then, a depeless-process for 25 minutes, and  
(3) a dry cleaning process for 15 minutes after adding a small amount of  $CF_4$ .

25 Figs. 4, 5 and 6 illustrate experimental results under the above processing conditions (1), (2) and (3),

respectively. In Figs. 4 to 6, vertical axis represents the intensity of photoelectron (arbitrary unit) and the horizontal axis represents the binding energy (in eV).

5 All the dry cleaning processes in the experiments under an exemplary processing condition below:

a pressure in the experimental chamber 202; 100 mTorr,  
a high frequency power applied to the bottom electrode  
and time during which the high frequency power is applied;  
2000 W and 1 minute, respectively,

10 a flow rate of O<sub>2</sub> gas supplied as the process gas; 700 sccm,

temperatures of the top electrode, the sidewall of the chamber and the bottom electrode; 60°C, 60°C and 40°C, respectively, and

15 pressure levels of a backgas (He); 7 Torr in the central region of an object to be processed and 40 Torr in the peripheral region thereof. Silicon dummy wafers were used in the dry cleaning process.

20 The depoless-process in the processing condition (2) was executed under a processing condition as follows:

a pressure in the chamber; 45 mTorr,  
a high frequency power applied to the bottom electrode  
and time during which the high frequency power is applied;  
1400 W and 1 minute, respectively,

25 flow rates of CF<sub>4</sub>, O<sub>2</sub> and Ar gases in a mixed gas thereof supplied as the process gas; 80 sccm, 20 sccm and

160 sccm, respectively,

temperatures of the top electrode, the sidewall of the chamber and the bottom electrode; 60°C, 60°C and 40°C, respectively, and

5        pressure levels of a backgas (He); 7 Torr in the central region of an object to be processed and 40 Torr in the peripheral region thereof.

In the processing condition (3), a CF<sub>4</sub> gas is provided at a flow rate of 2 sccm along with an O<sub>2</sub> gas. The CF<sub>4</sub> gas  
10        used herein serves to etch the silicon dummy wafer.

In the analysis of the XPS employed in the experiments, a peak of photoelectron intensity is detected at a specific binding energy of an element being analyzed. Thereafter, it can be deduced that the element whose peak appears in the  
15        XPS data is attached on the surface of the chip 200.

Fig. 4 illustrates an analysis result on the surface of the chip 200 prepared under the processing condition (1), which shows peaks of photoelectron intensity, especially for the oxygen element O and the silicon element Si.

20        Fig. 5 illustrates an analysis result on the surface of the chip 200 under the processing condition (2), which shows peaks of photoelectron intensity, especially for the fluorine element F and the yttrium element Y.

Fig. 6 illustrates an analysis result on the surface  
25        of the chip 200 under the processing condition (3), which shows peaks, especially for the fluorine element F and the

yttrium element Y as in the processing condition (2).

Since the surfaces of the chips 200 analyzed by XPS are formed of yttrium oxide ( $Y_2O_3$ ), peaks of photoelectron intensity corresponding to the yttrium element Y and the oxygen element O should be detected by the XPS analysis if the chip surfaces are not covered by deposits.

However, under the processing condition (1), there is no peak of photoelectron intensity corresponding to yttrium element Y, but there is shown a peak of photoelectron intensity corresponding to silicon element Si. Therefore, under the processing condition (1), it is believed that silicon sputter materials including silicon oxide  $SiO_2$  are attached on the surface of the chip 200.

Under the processing condition (2), there is shown a peak of photoelectron intensity corresponding to fluorine element F, instead of oxygen element O, and there is no peak of photoelectron intensity corresponding to silicon element Si. Therefore, under the processing condition (2), it is believed that the surface of the chip 200 is fluorinated so that the silicon sputter materials are removed by the depoleless-process.

Under the processing condition (3), there is shown a peak of photoelectron intensity corresponding to fluorine element F, instead of oxygen element O, and there is no peak of photoelectron intensity corresponding to silicon element Si. Therefore, under the processing condition (3), it is

believed that the surface of the chip 200 is fluorinated and there is no deposits of silicon sputter materials.

Referring to Figs. 7A to 7C, there are shown influences on variations in the etching rate and the in-  
5 surface uniformity of etching rate due to an additional amount of  $\text{CF}_4$  added during the dry etching process.

Figs. 7A to 7C are graphic illustration explaining variations in the etching rate and those in the in-surface uniformity of etching rate for cases where 25 wafers were  
10 treated with the depoless-process as shown in the previous embodiment after being treated by the dry cleaning process for 30 minutes. The vertical axes in graphs on the upper side represent an etching rate ( $\text{\AA}/\text{min}$ ); those on the lower side, an in-surface uniformity of etching rate (%); and the  
15 horizontal axes, an elapsed time (min) measured from the time of the termination of the dry cleaning process. The processing time of the depoless-process is about 1 minute per a wafer W and the number in the horizontal axes corresponds to the number of wafers processed by the  
20 depoless-process.

Figs. 7A to 7C correspond to cases of performing a dry cleaning process for 15 minutes, a dry cleaning process for 15 minutes with a polyimide attached on a surface of a wafer and a dry cleaning process for 30 minutes with a small  
25 amount of  $\text{CF}_4$  added (a flow rate of 2 sccm), respectively. Values shown in each graph denotes an average and a standard

deviation of an etching rate or an in-surface uniformity after the etching rate or the in-surface uniformity during the depoleless-process reaches a stable range. The stable ranges were determined based on the criteria that the etching rates and the in-surface uniformities respectively remain within  $\pm 1.0 \%$  and  $\pm 3.0 \%$  with respect to an average of the etching rates and an average of the in-surface uniformities after reaching their respective stable regions. The dotted portions in Figs. 7A to 7C represent unstable regions.

An exemplary processing condition of the depoleless-process for plasma-etching a thermal silicon oxide film formed all over the surface of the wafer, i.e., an object to be processed, with a diameter of 200 mm is processed by plasma etching is as follows:

- a pressure in the chamber; 45 mTorr,
- a high frequency power applied to the bottom electrode and time during which the high frequency power is applied; 1400 W and 1 minute, respectively,
- flow rates of  $\text{CF}_4$ ,  $\text{O}_2$  and Ar gases in a mixed gas thereof supplied as the process gas; 80 sccm, 20 sccm and 160 sccm, respectively,
- temperatures of the top electrode, the sidewall of the chamber and the bottom electrode;  $60^\circ\text{C}$ ,  $60^\circ\text{C}$  and  $40^\circ\text{C}$ , respectively, and
- pressure levels of the backgas (He); 7 Torr in a

central region of the object to be processed and 40 Torr in a peripheral region thereof.

Further, an exemplary processing condition for the dry cleaning process were as follows:

- 5           a pressure in the chamber; 100 mTorr,
- a high frequency power applied to the bottom electrode and time during which the high frequency power is applied; 2000 W and 1 minute, respectively,
- a flow rate of O<sub>2</sub> gas supplied as the process gas; 700
- 10       sccm,

temperatures of the top electrode, the sidewall of the chamber and the bottom electrode; 60°C, 60°C and 40°C, respectively, and

- pressure levels of a backgas (He); 7 Torr in the
- 15       central region of the object to be processed and 40 Torr in the peripheral region thereof. The silicon dummy wafers were used during the dry cleaning process.

Fig. 7A illustrates a case for performing dry cleaning process for 30 minutes. As soon as the dry cleaning process

20       was terminated after 30 minutes, the etching rate dropped and it took 9 minutes for the etching rate and the in-surface uniformity of etching rate to be stabilized. Fig. 7B illustrates a case for performing dry cleaning process for 30 minutes on a wafer with a polyimide film attached on

25       surface thereof. As soon as the dry cleaning process was terminated after 30 minutes, the etching rate also dropped



and the stabilization time for the etching rate reduced to 6 minutes. Further, it took 9 minutes for the in-surface uniformity to be stabilized. From this, it is speculated that the silicon wafer with the surface thereof coated with a polyimide film suppresses the generation and accumulation of silicon sputter materials. Fig. 7C illustrates a case for performing dry cleaning process for 30 minutes with a small amount of  $\text{CF}_4$  (a flow rate of 2 sccm) added. After the dry cleaning process is completed, the etching rate did not drop and remained approximately constant. The in-surface uniformity reduced slightly but it takes 1 minute for the in-surface uniformity to be stabilized.

From the experimental results described above, it is evident that the decrease of the etching rate in the depoless-process right after the dry cleaning process largely resulted from the silicon sputter materials such as silicon oxide attached in the chamber during the dry cleaning process.

Further, it appears that the accumulation of silicon sputter materials is suppressed and therefore the drop of the etching rate in the depoless-process right after the dry cleaning process is also suppressed, by adding a small amount of  $\text{CF}_4$  functioning to etch the silicon dummy wafer during the dry cleaning process.

Figs. 8A to 8D illustrate results to examine an appropriate amount of  $\text{CF}_4$  to be added in the dry cleaning

process to obtain the effects described above.

Figs. 8A to 8D are graphic illustrations explaining variations in the etching rate and those in the in-surface uniformity (%) of etching rate for cases where 25 sheets of wafers treated with the depoless-process as shown in the previous embodiment after being treated by the dry cleaning process for 30 minutes. The vertical axes in graphs on the upper side represent an etching rate ( $\text{\AA}/\text{min}$ ); those on the lower side, an in-surface uniformity of etching rate (%); and the horizontal axes, an elapsed time (min) measured from the time of the termination of the dry cleaning process. The processing time of the depoless-process is about 1 minute per a wafer W and the number in the horizontal axes corresponds to the number of wafers processed by the depoless-process.

Figs. 8A to 8D correspond to cases of performing a dry cleaning process for 30 minutes in which  $\text{CF}_4$  is added with the flow rates of 0.4 sccm, 2 sccm, 10 sccm and 50 sccm, respectively. Values shown in each graph denotes an average and a standard deviation of an etching rate or an in-surface uniformity after the etching rate or the in-surface uniformity during the depoless-process reaches a stable range. The stable ranges were determined based on the criteria that the etching rates and the in-surface uniformities respectively remain within  $\pm 1.0 \%$  and  $\pm 3.0 \%$  with respect to an average of the etching rates and an

average of the in-surface uniformities after reaching their respective stable regions. The dotted portions in Figs. 8A to 8D represent unstable regions.

5 An exemplary processing condition of the depoless-process for plasma-etching a thermal silicon oxide film formed all over the surface of the wafer, i.e., an object to be processed, with a diameter of 200 mm is processed by plasma etching is as follows:

a pressure in the chamber; 45 mTorr,  
10 a high frequency power applied to the bottom electrode and time during which the high frequency power is applied; 1400 W and 1 minute, respectively,

flow rates of  $\text{CF}_4$ ,  $\text{O}_2$  and Ar gases in a mixed gas thereof supplied as the process gas; 80 sccm, 20 sccm and  
15 160 sccm, respectively,

temperatures of the top electrode, the sidewall of the chamber and the bottom electrode;  $60^\circ\text{C}$ ,  $60^\circ\text{C}$  and  $40^\circ\text{C}$ , respectively, and

pressure levels of the backgas (He); 7 Torr in a  
20 central region of the object to be processed and 40 Torr in a peripheral region thereof.

Further, an exemplary processing condition for the dry cleaning process were as follows:

a pressure in the chamber; 100 mTorr,  
25 a high frequency power applied to the bottom electrode and time during which the high frequency power is applied;

2000 W and 1 minute, respectively,

a flow rate of O<sub>2</sub> gas supplied as the process gas; 700 sccm,

temperatures of the top electrode, the sidewall of the chamber and the bottom electrode; 60°C, 60°C and 40°C, respectively, and

pressure levels of a backgas (He); 7 Torr in the central region of the object to be processed and 40 Torr in the peripheral region thereof. The silicon dummy wafers were used during the dry cleaning process.

Referring to Figs. 8A to 8D, when the flow rate of CF<sub>4</sub> added during the dry cleaning process was 0.4 sccm, it was observed that the etching rate and the in-surface uniformity of etching rate dropped and it took 4 minutes the etching rate and the in-surface uniformity of etching rate to be stabilized. When the flow rate of CF<sub>4</sub> was not less than 2 sccm, the etching rate did not drop; and the in-surface uniformity reduced slightly but it took 1 to 2 minutes for in-surface uniformity of etching rate to be stabilized. Thus, it is clear that the drop of the etching rate after the dry cleaning process can be suppressed if the oxygen gas and CF<sub>4</sub> are simultaneously supplied at flow rates of 700 sccm and not less than 2 sccm during the dry cleaning process, respectively.

However, if a flow rate of CF<sub>4</sub> becomes unnecessarily large, all parts in the plasma processing apparatus may be

5        rusted. Therefore, the ratio of flow rate of oxygen to that  
of  $\text{CF}_4$  during the dry cleaning process is preferably not  
less than 700 sccm / 1 sccm (about 0.14 %) but not greater  
than 700 sccm / 50 sccm (about 7.1 %), and more preferably  
not less than 700 sccm / 2 sccm (about 0.29 %) but not  
greater than 700 sccm / 10 sccm (about 1.4 %).

10        Another experiment performed to examine a dependence  
of the variations of the etching rate on other conditions  
during the dry cleaning process will be described. As shown  
in Fig. 9, a plurality of resist chips were attached on a  
ceiling plate 302, a sidewall (deposition shield) 304, an  
insulator ring 310 and a baffle plate 312 of an experimental  
chamber 300 by using a silicone tape (not shown) having a  
good thermal conductivity. And then the dry cleaning  
15        process was performed under various conditions to examine a  
dependence of a variation of an ashing rate and an ashing  
time on (1) the presence of  $\text{CF}_4$  added (when added, a  $\text{CF}_4$   
flow rate was 2 sccm) and (2) a magnitude of power applied  
to the bottom electrode.

20        A wafer W was mounted on a supporting table 306 in the  
experimental chamber 300 and a focus ring 308 was disposed  
around an upper periphery of the supporting table 306 to  
converge plasma in a processing space S. The focus ring 308  
was made of a conductive material, e.g., single crystalline  
25        silicon. Installed around the outer periphery of the focus  
ring 308 was an insulator ring 310 of, e.g., silicon oxide.

Installed around the lower portion of the experimental chamber 300 was a baffle plate 312.

As shown in Fig. 10, the resist chips were attached on the following portions inside the experimental chamber 300:

5           ① on a central portion of a ceiling plate corresponding to a portion right above the central port of the wafer W,

          ② on a portion of the ceiling plate located 50 mm apart from the central portion thereof,

10          ③ on a portion of the ceiling plate located 95 mm apart from the central portion thereof,

          ④ on a portion of the ceiling plate located 140 mm apart from the central portion thereof,

15          ⑤ on a portion of the deposition shield located 50 mm apart (near the top thereof) from the bottom surface of the experimental chamber,

          ⑥ on a portion of the deposition shield located 40 mm apart from the bottom surface of the experimental chamber,

20          ⑦ on a portion of the deposition shield located 30 mm apart from the bottom surface of the experimental chamber,

          ⑧ on a portion of the deposition shield located 20 mm apart from the bottom surface of the experimental chamber,

25          ⑨ on a portion of the deposition shield located 10 mm apart (near the bottom thereof) from the bottom surface of the experimental chamber,

          ⑩ on the insulator ring,

- ⑪ on the baffle plate near the supporting table,
- ⑫ on the baffle plate at the center thereof, and
- ⑬ on the baffle plate near the sidewall.

In order to examine the influence due to an addition  
5 of CF<sub>4</sub> (with a flow rate of 2 sccm when added), the dry  
cleaning process was performed under the following  
condition:

- a pressure in the chamber 300; 100 mTorr,
- a high frequency power applied to the bottom electrode  
10 and time during which the high frequency power is applied;  
1500 W and 1 minute, respectively,
- flow rate of O<sub>2</sub> supplied as the process gas; 700 sccm,
- temperatures of the top electrode, the sidewall of the  
chamber and the bottom electrode; 60°C, 60°C and 40°C,  
15 respectively, and
- pressure levels of a backgas (He); 7 Torr at the  
central region of the object to be processed and 40 Torr at  
the peripheral region thereof.

In order to examine the influence due to a variation  
20 in a magnitude of power applied to the bottom electrode, the  
dry cleaning process was performed under the following  
condition:

- a pressure in the chamber 300; 100 mTorr,
- a high frequency power applied to the bottom electrode  
25 and time during which the high frequency power is applied;  
1500 W and 1 minute, respectively,

a ratio of flow rate of O<sub>2</sub> gas to that of CF<sub>4</sub> gas supplied as the process gas; 700 sccm / 2 sccm,

temperatures of the top electrode, the sidewall of the chamber and the bottom electrode; 60°C, 60°C and 40°C, respectively, and

a pressure range of a backgas (He); 7 Torr at the central region of the object to be processed and 40 Torr at the peripheral region thereof.

Fig. 10 is a table of the result of the experiment 1) describing a relationship between the presence of CF<sub>4</sub> added and the ashing rate (Å/min) at each location in the experimental chamber 300. As can be seen from Fig. 10, all the maximum (Max.), the minimum (Min.), the average (Ave.) and the uniformity (Unif.) of the ashing rate do not vary much regardless of whether a small amount of CF<sub>4</sub> is added or not. The uniformity (Unif.) is defined by  $(\text{Max.} - \text{Min.}) / (2 \times \text{Ave.}) \times 100$ . Since there are no significant variations in the ashing rate of the resist due to the addition of CF<sub>4</sub>, it may be deduced that there will be no significant variations in the etching rate due to the addition of CF<sub>4</sub> as well.

Fig. 11 is a table of the result of the experiment 2) describing a relationship between a power (W) applied to the bottom electrode and time (second) required to remove the deposits attached to the resist chip at each location in the experimental chamber 300 after completing the depo-process for 25 wafers with a processing time of 3 min/wafer. The



powers applied to the bottom electrode were 500W, 1000W and 1500W, respectively.

As can be seen from Fig. 11, all of a maximum (Max.), a minimum (Min.) and an average (Ave.) of the ashing time required for ashing are reduced at each location of the experimental chamber as the power applied to the electrode increases from 500 W to 1500 W. Accordingly, it may be deduced that the ashing rate increases in proportion to the power applied to the bottom electrode.

However, if the applied power increases from 500 W to 1000 W, an uniformity (Unif.) in time required for ashing reduces. On the other hand, if the applied power increases from 1000 W to 1500 W, the uniformity in time required for ashing slightly increases from 116.68 to 117.92. Accordingly, it can be deduced that, if the power applied to the bottom electrode is larger than a certain value, the uniformity of the ashing rate is deteriorated. The uniformity (Unif.) is  $(\text{Max.} - \text{Min.}) / (2 \times \text{Ave.}) \times 100$ .

If the high frequency power applied to the bottom electrode is excessively increased, the temperature in the experimental chamber 300 also excessively increases, which would affect each part in the plasma processing apparatus 100.

Therefore, in case of the apparatus having the configuration described above, it is preferable that the power applied to the bottom electrode ranges from 1000 W to

1500 W (from about 3.18 W/cm<sup>2</sup> to about 4.78 W/cm<sup>2</sup>) during the ashing process on the resist chips. Therefore, it is also preferable that the applied power during the etching process is identical to the power range described above.

5           Through the repeated experiments on the dry cleaning process of the plasma processing, it has been found that by supplying both a deposit removing gas including O<sub>2</sub> and a dummy wafer etching gas (dummy substrate etching gas) including CF<sub>4</sub> into the chamber, a deposition film, e.g., a  
10 silicon sputter materials, is prevented from being deposited on a, e.g., sidewall in the plasma processing apparatus.

          Accordingly, as shown in Figs. 12A and 12B, the dry cleaning process of the plasma processing in accordance with the present invention is different from the conventional dry  
15 cleaning process. Specifically, the dry cleaning process of the present invention is performed with a small amount of CF<sub>4</sub> added in the process gas. Therefore, the dry cleaning process of the present invention does not require a seasoning process thereafter and, thus, additional efforts  
20 and time for the seasoning process can be saved and a series of plasma processes can be realized with an improvement in operating rate thereof.

          Even though the preferred embodiments of the present invention have been described in conjunction with the  
25 accompanying drawings, the present invention is not limited thereto.

Even though, for example, the etching is described as the plasma processing in preferred embodiments of the invention, the plasma processing is not limited to the etching. Rather, same effects may be achieved in other plasma processing, e.g., ashing, sputtering and the like, if deposits including silicon sputter materials have an adverse effect on the plasma processing.

Further, even though a small amount of  $\text{CF}_4$  is used as the dummy wafer etching gas (dummy substrate etching gas) added to the deposit removing gas during the dry etching process in accordance with the preferred embodiments of the invention, any other gas capable of etching the wafer by reacting with it may be used as the dummy wafer etching gas. Specifically, a CF based gas other than  $\text{CF}_4$ , a CHF based gas or a SF based gas may be used as the dummy wafer etching gas.

Furthermore, though  $\text{O}_2$  is used as the deposit removing gas during the dry etching process in accordance with the preferred embodiment of the present invention, any other gas may be used as the deposit removing gas as long as such gas is capable of forming a compound to be evaporated with a high vapor pressure by reacting with the deposits of the deposition film to be eliminated. Specifically, a nitrogen gas, a hydrogen gas, an ammonia gas or a mixed gas of a combination thereof may be used as the deposit removing gas.

Moreover, though the high frequency power is applied to the bottom electrode, i.e., the supporting table, and the

top electrode, i.e., the shower head, is grounded in the  
embodiments of the present invention, the same effects may  
be obtained in case the high frequency power is applied to  
the top electrode, i.e., the shower head, and the bottom  
5 electrode, i.e., the supporting table, is grounded.

Since the deposits such as silicon sputter materials  
are prevented from being accumulated on the wall inside the  
chamber during the dry cleaning process in accordance with  
the present invention as described above, the etching rate  
10 can be prevented from being dropped right after the dry  
cleaning process. As a result, the conventional seasoning  
process carried out right after the dry cleaning process in  
order to execute the depoless-process becomes unnecessary  
and the additional effects and time for the seasoning  
15 process may be eliminated, enabling a series of plasma  
processes to be realized with an improvement in the  
operating rate thereof.

While the invention has been shown and described with  
respect to the preferred embodiments, it will be understood  
20 by those skilled in the art that various changes and  
modifications may be made without departing from the spirit  
and scope of the invention as defined in the following  
claims.